RESEARCHERID
THOMSON REUTERS

[ICESTM-2018]

ISSN 2348 – 8034
Impact Factor- 5.070

GLOBAL JOURNAL OF ENGINEERING SCIENCE AND RESEARCHES

DESIGN OF SERIES VOLTAGE COMPENSATOR TO REDUCE DC-LINK CAPACITANCE FOR INDUCTION MOTOR DRIVE

Rajesh Pamarthi[*1] & Sri. P. Ankineedu Prasad[2]

[*1]M-Tech - EPS Student Scholar, Department of Electrical & Electronics Engineering, Vikas Group of Institutions, Nunna, Vijayawada, Krishna (Dt), A.P, India.

[2]Associate Professor, Department of Electrical & Electronics Engineering, Vikas Group of Institutions, Nunna, Vijayawada, Krishna (Dt), A.P, India.

ABSTRACT

In this paper Design of Series Voltage Compensator for Reduction of DC-Link Capacitance in Grid-Tie Solar Inverter is proposed. A grid-tie solar inverter with a series voltage compensator for reducing the high-voltage dc-link capacitance is presented. The compensator obtains energy from the dc link to sustain the voltage on its dc side and generates an ac voltage to counteract the voltage ripple on the dc link. As the compensator processes small ripple voltage on the dc link and reactive power, it can be implemented with low-voltage devices, and thus, its volt amp rating is small. As the required energy storage of the dc link, formed by a reduced value of the dc-link capacitor and the compensator, is reduced, the architecture allows replacing popularly used electrolytic capacitors with alternatives of longer lifetime, such as power film capacitors, or extending the system lifetime even if there is a significant reduction in the capacitance of electrolytic capacitors due to aging. Detailed mathematical analysis on the static and dynamic behaviors of the overall system, and the control method will be presented. The simulation results are presented by using Matlab/Simulink system.

Keywords: *Capacitors, capacitor-supported systems, dc–ac power conversion, grid-tie solar inverters, photovoltaic systems, reliability.*

I. INTRODUCTION

A capacitor-supported system consists of multiple power converters interconnected by a dc link. The dc-link voltage is maintained by a capacitor bank that absorbs instantaneous power difference between the input source and output load, minimizing voltage variation on the dc link, and providing sufficient energy during the hold-up time of the system. Among different types of capacitor, aluminum electrolytic capacitors (E-Caps) are the most popular choice because of their high volumetric efficiency and low cost. However, they suffer from the drawbacks of high equivalent series resistance (ESR); low ripple current capability; bottleneck of the voltage rating; relatively short lifetime compared to other components; and considerable maintenance work. Advances in power film capacitor technology are emerging for dc-link filtering [1], [2]. Power film capacitors outperform aluminum E-Caps in terms of ESR, self-healing capability, life expectancy, environmental performance, dc-blocking capability, ripple current capability, and reliability. Although low-voltage and high-value film capacitors are available, the capacitance of the high-voltage film capacitors still cannot compete with E-Caps, due to their relatively low volumetric efficiency and high cost. To lessen the dependency of the dc-link capacitance, there are many prior-art methods, based on the following approaches:

1) Performance trade-off:- This method allows a larger voltage ripple across the dc link with a smaller capacitance. However, it is practically less impressive as the system performance will be degraded. It is more suitable for certain applications, like the ones in [3]–[5]. A set of design procedure is given in [6] for the optimization of capacitor bank.

2) Reduction of the dc-link capacitor current with sophisticated control: The concept is based on reducing the ripple current flowing through the dc-link capacitor [7]. The front-stage converter is an active rectifier, and a step-up dc–dc converter in [8], while the output is an inverter. Their key advantage is that no additional circuit is needed. However, those control methods cannot be applied to systems with front-end diode-bridge rectifier. Apart from requiring a sophisticated controller, some of them also rely on specific relationship in the operating frequency between the converters connected [9].

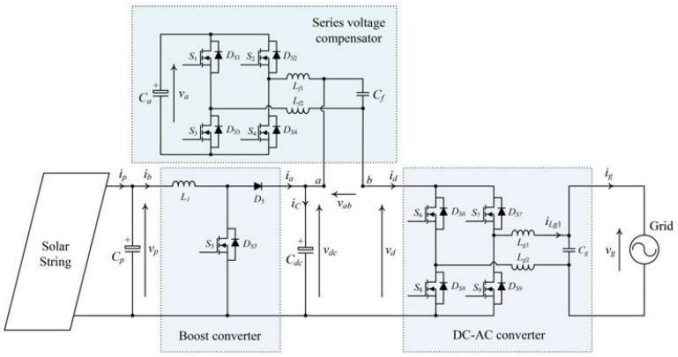
The method given is limited to three-phase systems. The controller described is based on assuming an ideal energy conversion. Thus, the actual input current would be distorted unless multiple cell load inverters are used. The performance of those controllers is greatly dependent on the accuracy of the computations [10] and affected by the overall time delays of the control loops.

3) Increase in the frequency of the dc-link voltage ripple: A double frequency front-end converter with multiphase switching is proposed in [11] to reduce the ripple voltage. However, the approach cannot reduce the dc-link capacitance significantly.

4) Ripple cancellation circuit with a coupled element: In [12], a coupled inductor is applied to cancel the voltage ripple of the dc input, dc output, or dc link of a power converter. The concept is based on assuming that the capacitor used in the storage tank is infinite. But in reality, the capacitance has a finite value, and the coupled inductor filter and the capacitor form a low-pass filter. To avoid large-sized coupled windings, the technique is more suitable for filtering high-frequency ripples or noise, such as switching ripple, EMI filtering. Moreover, the dynamic response of the capacitor may be degraded due to the series-connected coupled winding.Large electric drives will require advanced power electronic inverters to meet the high power demands (>1 MW) required of them. One inverter type which is uniquely suited for this application is the multilevel inverter [13]. Twodifferent multilevel converter topologies are ideal for use aslarge electric drives. The cascaded inverter with separate dc sources closely fits the needs of all-electric vehicles because it can use the onboard batteries or fuel cells to synthesize a sinusoidal voltage waveform to drive the main vehicle traction motor. Where generated ac voltage is available, a back-to-back diode clamped converter can be used to output variable frequency ac voltage for the driven motor [14].

II. OPERATION OF THE SERIES VOLTAGE COMPENSATOR

Fig. 1 shows the architecture of the grid-tie solar invertersystem with a series voltage compensator connected to the dclink. The system consists of two power conversion stages. Thefront stage is a dc–dc boost converter. It is connected betweena string of solar panels and the dc link. The output stage isa grid-tie dc–ac converter, which is connected between the dclink and the power grid. The compensator, which is a capacitorsupported full-bridge dc–ac converter without an external dcsource, is connected between the two converters. The voltagecompensator generates an ac voltage that counteracts the ripplevoltage on the output of the boost converter. Thus, the input ofthe grid-tie inverter is a dc voltage equal to the average value ofthe voltage vdc across the dc-link capacitor Cdc.The dc-link voltage vdc and the input voltage of the voltagecompensator va are sensed. The scaling factor α is the ratiobetween Vtric and Va,ref , where Vtric is the amplitude of thetriangular carrier signal vtric in the PWM controller and Va,refis the voltage reference for the input voltage of the voltagecompensator. The difference between Va,ref and va is processedby a PI controller G(s) to give an offset voltage vos. The controlsignal vcon is obtained by combining α vdc with vos. The dccomponent of α vdc is ideally cancelled in vcon by vos as Vos =−αVdc, where Vos and Vdcare the dc component of vos andvdc, respectively. With such arrangement, it is unnecessary touse a high-pass filter to extract the ac component of vdc. Atthe same time, the stable dc level of va can be obtained by



ISSN 2348 – 8034
Impact Factor- 5.070

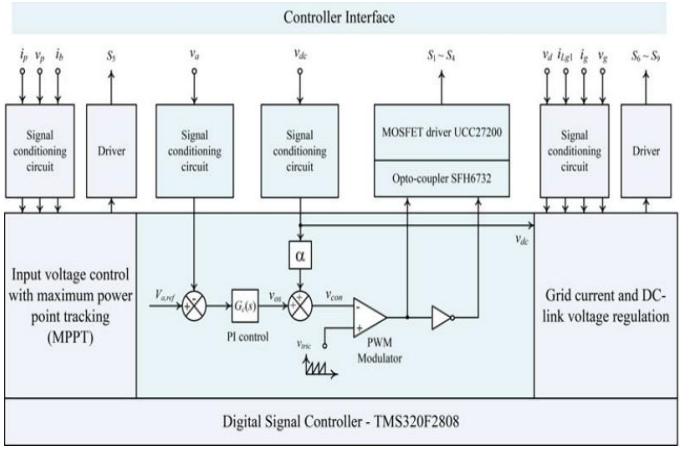


Fig. 1. Architecture of the grid-tie solar inverter with a series voltage compensator.

Voltage control, which ensures the compensator only handlesthe reactive power in the steady state. During the steady-stateoperation, vcon equals the conditioned ac component of αvdc. Itis then used to compare with the triangular carrier waveform inthe pulse width modulation modulator to generate the voltagevab having the same phase and amplitude with Δvdc. Withoutany external power supply, the power dissipation of the voltagecompensator is obtained from the dc link. Practically speaking,instead of a pure ac voltage, both vab and vcon consists of notonly ac component, but also small amount of the dc component.Since the input current of the grid-tie inverter consists of the dccomponent, some power will be absorbed by the compensator ifvab consists of the dc component. Derivations of the parametersin the control.

III. SYSTEM CHARACTERISTICS

The grid voltage vg and the output grid current ig can beexpressed as

$$v_g(t) = V_g \sin \omega t \tag{1}$$

$$i_g(t) = I_g \sin(\omega t + \phi) \tag{2}$$

Where Vg and Ig are the amplitude of vg and ig , respectively,ω = 2πf is the angular line frequency, f is the line frequency,and φ is the phase difference between vg and ig .Based on (1) and (2), the instantaneous output power pg is

$$\begin{aligned} p_g(t) &= v_g(t) i_g(t) \\ &= \frac{2P_g}{\cos \phi} \sin \omega t \sin(\omega t + \phi) \end{aligned} \tag{3}$$

Where Pg =VgIg/2 cos φ is the average output power.By applying the Kirchhoff's current law at the node of theDc-link capacitor Cdc, the relationship among the output currentia of the boost converter, the dc-link capacitor current iC, andinput current id of the inverter can be expressed as

$$i_C(t) = i_a(t) - i_d(t) \tag{4}$$

The dominant component of Δvdc is the double of the linefrequency harmonics. For the sake of simplicity in the analysis,Δvdc is expressed as

$$\Delta v_{\mathrm{dc}}(t) = |\Delta V_{\mathrm{dc}}| \sin(2\omega t + \theta) \quad (5)$$

Where |ΔVdc| is the magnitude of Δvdc and θ is the phase angleof Δvdc.

A. Steady-State Characteristics of the Voltage Compensator

Since the voltage compensator counteracts the ripple voltageon the dc-link capacitor only, the input voltage of the grid-tiedc–ac converter, vd, is equal to Vdc. By using (3), the inputcurrent of the dc–ac converter, id, can be expressed as

$$\begin{aligned} i_d(t) &= \frac{p_g(t)}{V_{\mathrm{dc}}} \\ &= \frac{P_g}{V_{\mathrm{dc}} \cos\phi} [\cos\phi - \cos(2\omega t + \phi)] \end{aligned} \quad (6)$$

By substituting (5) and (6) into (4),

$$\gamma \cos(2\omega t + \theta - \delta) = \frac{P_g}{\lambda V_{\mathrm{dc}} \cos\phi} \cos(2\omega t + \phi) \quad (7)$$

Where

$$\gamma = \sqrt{\left(\frac{P_g}{V_{\mathrm{dc}}}\right)^2 + (2\omega C_{\mathrm{dc}} V_{\mathrm{dc}})^2}, \delta = \tan^{-1}\left(\frac{P_g}{2\omega C_{\mathrm{dc}} V_{\mathrm{dc}}^2}\right)$$

and λ = |ΔVd c | /Vd c is the ripple factor.

Detailed proof of (7) is given in the Appendix.By equating the magnitude and phase angle of the LHS andRHS of (7), the following equations can be concluded

$$\begin{aligned} |\Delta V_{\mathrm{dc}}| &= \frac{P_g}{\gamma \cos\phi} \\ \theta &= \phi + \delta. \end{aligned} \quad (8)$$

By substituting (8) into (5), the ripple voltage on the dc-linkcapacitor is

$$\begin{aligned} \Delta v_{\mathrm{dc}}(t) &= \frac{P_g}{\gamma \cos\phi} \sin(2\omega t + \phi + \delta) \\ &= \lambda V_{\mathrm{dc}} \sin(2\omega t + \phi + \delta). \end{aligned} \quad (9)$$

According to (9), the relationship among the dc-link capacitance Cdc, output phase angle φ, and the ripple factor λ is

$$C_{\mathrm{dc}} = \frac{S_g}{2\omega V_{\mathrm{dc}}^2} \sqrt{\frac{1}{\lambda^2} - \cos^2\phi} \quad (10)$$

Where Sg is the apparent power of the solar inverter.Detailed proof of (10) is given in the Appendix.

ISSN 2348 – 8034
Impact Factor- 5.070

Thus, for a given apparent power Sg , the required value ofCdc will increase as the power factor cos φ decreases. Thus, oneof the design constraints is based on considering the minimumpower factor. For example, as stated in the statutory requirementVDE-AR-N 4105, the minimum power factor is 0.9.As the compensator handles ripple voltage only (i.e., vab =Δvdc), the ratio between the apparent power handled by thecompensator, Sab, and the apparent power of the whole systemis

$$\frac{S_{ab}}{S_g} = \frac{v_{ab,\mathrm{rms}} i_{d,\mathrm{rms}}}{v_{d,\mathrm{rms}} i_{d,\mathrm{rms}}} = \frac{|\Delta V_{\mathrm{dc}}|}{\sqrt{2} V_{\mathrm{dc}}} \tag{11}$$

where vab,rms and vd,rms are the rms values of vab and vd,respectively, and id,rms is the rms value of the input current ofthe dc–ac converter.Thus, as ΔVdc Vdc, the power rating of the compensatoris much smaller than that of the whole system.The voltage across the capacitor Ca, va, is regulated at Va,refby using the control mechanism depicted in Fig. 1. If va<Va,ref ,energy will be absorbed from the dc link, and vice versa. Whenva=Va,ref , the voltage compensator will ideally absorb zeropower. Based on (6) and (9), the average power absorbed by thevoltage compensator Pab is

$$\begin{aligned} P_{ab} &= \frac{1}{T} \int_0^T v_{ab}(t) i_d(t) dt \\ &= -\frac{P_g^2 \sin \delta}{2\gamma V_{\mathrm{dc}} \cos^2 \phi} \end{aligned} \tag{12}$$

Where the period T = π / ω.
Thus, based on (12), if the compensator only generates theripple voltage on the dc-link capacitor, it will generate activepower. In order to maintain the power balance for stabilizing vaat Va,ref , a small voltage offset at vab, Vab, appears

$$\begin{aligned} V_{ab} &= \frac{-P_{ab}}{I_d} \\ &= \frac{P_g \sin \delta}{2\gamma \cos^2 \phi} \end{aligned} \tag{13}$$

The relationship between vab and va can be expressed as

ISSN 2348 – 8034
Impact Factor- 5.070

$$v_{ab}(t) = \frac{v_{\text{con}}(t)}{V_{\text{tric}}} v_a(t)$$
$$= \frac{\alpha v_{\text{dc}}(t) + v_{\text{os}}(t)}{V_{\text{tric}}} v_a(t)$$
$$= \frac{\alpha P_g}{\gamma V_{\text{tric}} \cos\phi} \sin(2\omega t + \phi + \delta) v_a(t)$$
$$+ \frac{\alpha V_{\text{dc}} + v_{\text{os}}(t)}{V_{\text{tric}}} v_a(t). \quad (14)$$

The first term αPg sin(2ωt+φ+δ)γVtric cos φ va(t) represents the ripplevoltage compensation on the dc-link capacitor. The second termαVd c +vo s (t)Vtric va(t) represents the dc component, related to thepower balance described in (13). Thus, asymmetrical PWMswitching occurs.Fig. 2(a) and (b) present the operating modes of the compensator using a full bridge. When S2 and S3 are on, the capacitorCais charged by the load current id. Conversely, when S1 andS4 are on, the capacitor Ca is discharged by id. Fig. 2(c) showsthe waveforms of the dc- link capacitor voltage vdc, modulatingsignal vm , triangular carrier signal vtric, and the voltage acrossCa, va.The dc component on vab is very small. It is observedto be 2.1 V, about 0.5% of the average dc-link voltage of400 V in the 2-kW inverter system, which will be described. Thus, such dc component is neglected in the following discussion.

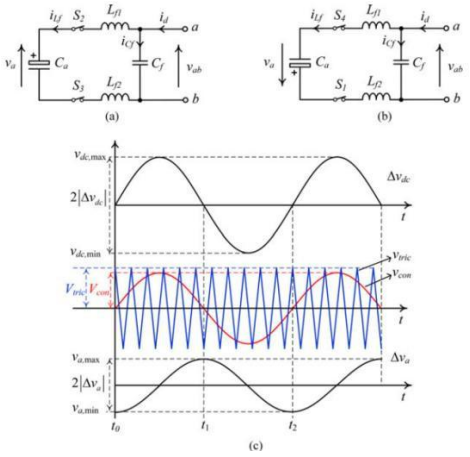


Fig. 2. Ripple voltage on the input capacitor Ca in the compensator. (a) Operation when S2 and S3 are on. (b) Operation when S1 and S4 are on. (c) SPWM andthe ripple voltage generated across Ca .

During the time interval between the time instants t0 and t1 inFig. 2(c), Ca is charged by the load current. By using (6) and (9)

ISSN 2348 – 8034
Impact Factor- 5.070

$$\begin{aligned} & v_a(t) \\ & = v_{a,\min} + \frac{1}{C_a}\int_{t_0}^{t_1} [i_d(t) - i_{Cf}(t)]\frac{v_{\text{con}}(t)}{V_{\text{tric}}}dt \\ & = v_{a,\min} \\ & \quad + \frac{1}{C_a}\int_{t_0}^{t_1} \left\{\frac{P_g}{V_{\text{dc}}\cos\phi}[\cos\phi - \cos(2\omega t + \phi)] - i_{Cf}(t)\right\} \\ & \quad \times \frac{\alpha P_g}{\gamma V_{\text{tric}}\cos\phi}\sin(2\omega t + \phi + \delta)dt \end{aligned} \tag{15}$$

Where va,min is the minimum voltage of va.
From t0 to t1, the net charge on the output filter capacitor Cfis zero. Only the double frequency component of the voltage onCais considered. Based on (15), the peak-peak voltage on Ca,2|ΔVa|, is

$$2\,|\Delta V_a| = \frac{\alpha P_g^2}{\gamma\omega C_a V_{\text{dc}} V_{\text{tric}}\cos\phi} \tag{16}$$

Thus, the voltage on Ca is

$$v_a(t) = V_a - \frac{\alpha P_g^2}{2\gamma\omega C_a V_{\text{dc}} V_{\text{tric}}\cos\phi}\cos(2\omega t + \phi + \delta) \tag{17}$$

Hence, the ripple voltage on the input of the voltage compensator is dependent on the values of Ca and Cdc. The guidelines for designing their values will be discussed later. Finally, based on (9), the voltage across Cdc, vdc, and the current through Cdc, iC , are

$$v_{\text{dc}}(t) = V_{\text{dc}} + \frac{P_g}{\gamma\cos\phi}\sin(2\omega t + \phi + \delta) \tag{18}$$

$$\begin{aligned} i_C(t) &= C_{\text{dc}}\frac{dv_{\text{dc}}(t)}{dt} \\ &= \frac{2\omega C_{\text{dc}} P_g}{\gamma\cos\phi}\cos(2\omega t + \phi + \delta) \end{aligned} \tag{19}$$

The maximum voltage across Cdc, Vdc,max, and the rms current through Cdc, IC,rms, are

$$V_{\text{dc,max}} = V_{\text{dc}} + \frac{P_g}{\gamma\cos\phi} \tag{20}$$

$$I_{C,\text{rms}} = \frac{\sqrt{2}\omega C_{\text{dc}} P_g}{\gamma\cos\phi} \tag{21}$$

B. Steady-State Characteristics of the Boost Converter
The voltage conversion ratio gb(t) of the front-stage boost converter is

$$g_b(t) = \frac{v_{\text{dc}}(t)}{v_p(t)}$$

ISSN 2348 – 8034
Impact Factor- 5.070

$$= \frac{V_{\mathrm{dc}} + \Delta v_{\mathrm{dc}}(t)}{v_p(t)} \tag{22}$$

Where vp(t) is the input voltage of boost converter.
Under the steady-state operation, vp should be relatively constant in order to ensure that the solar string is controlled to operate at a stable operating point (normally at the maximum power point). Thus, based on (22), the duty cycle db(t) of the main switch S5 in the boost converter is

$$d_b(t) = 1 - \frac{V_p}{V_{\mathrm{dc}}\left[1 + \lambda \sin(2\omega t + \phi + \delta)\right]} \tag{23}$$

Where Vp is the amplitude of vp. Hence, the average duty cycle of S5, Db, is

$$D_b = 1 - \frac{V_p}{V_{\mathrm{dc}}} \tag{24}$$

By substituting (24) into (23)

$$d_b(t) = 1 - (1 - D_b)\frac{V_{\mathrm{dc}}}{v_{\mathrm{dc}}(t)} \tag{25}$$

Based on (22), the minimum conversion ratio of the boost converter, gb,min, is unity. Thus

$$g_{b,\min} = \frac{V_{\mathrm{dc}}(1 - \lambda_{\max})}{V_{p\_\max}} = 1 \tag{26}$$

Where Vp max is the maximum input voltage of boost converter or the maximum voltage delivered by the solar string. Thus, based on (26), the maximum value of λ, λmax, is

$$\lambda_{\max} = 1 - \frac{V_{p\_\max}}{V_{\mathrm{dc}}}$$

By substituting (27) into (10), the minimum value of the dc-link capacitance, Cdc min, for a front-end boost converter is

$$C_{\mathrm{dc\_min}} = \frac{P_g}{2\omega V_{\mathrm{dc}}^2}\sqrt{\frac{1}{\left(1 - \frac{V_{p\_\max}}{V_{\mathrm{dc}}}\right)^2} - 1} \tag{28}$$

C. Small-Signal Dynamical Modeling
The solar string is modeled by a resistor Req. The boost converter, compensator, and the dc–ac converter are modeled by using the averaged ac modeling technique described. Their small-signal models and control block diagrams are shown in Figs. 3–5 the small-signal model of the whole system in Fig. 1 is shown in Fig. 6. Based on, the small-signal equation for the solar stringIs

$$\Delta V_p(s) = -R_{\mathrm{eq}}\Delta I_p(s) \tag{29}$$

ISSN 2348 – 8034
Impact Factor- 5.070

For the boost converter, the small-signal equations are given as follows:

$$\Delta V_p(s) - sL_1\Delta I_p(s) + V_{\rm dc}\Delta D_b(s) - (1-D_b)\Delta V_{\rm dc}(s) = 0 \quad (30)$$

$$(1-D_b)\Delta I_p(s) - I_p\Delta D_b(s) - \Delta I_a(s) = 0 \quad (31)$$

$$\Delta D_b(s) = \frac{1}{V_{\rm trib}} G_b(s)\Delta V_p(s) \quad (32)$$

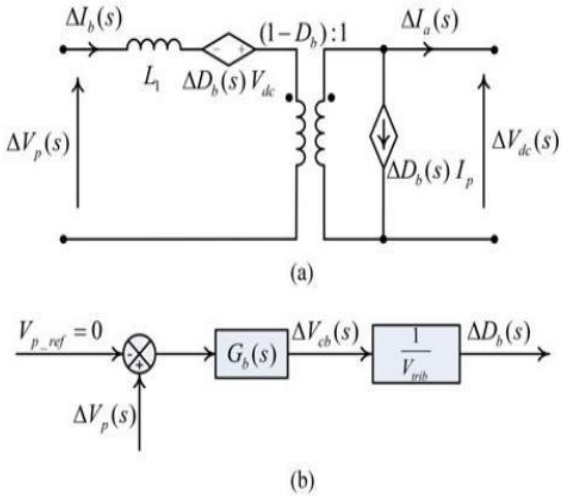


Fig. 3. Modeling of the boost converter. (a) Power stage. (b) Control block diagram.

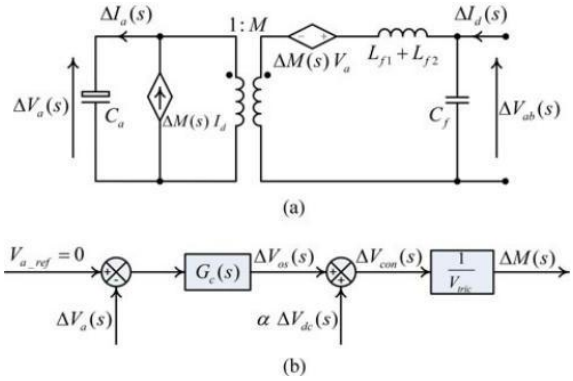


Fig. 4. Modeling of the compensator. (a) Power stage. (b) Control block diagram.

ISSN 2348 – 8034
Impact Factor- 5.070

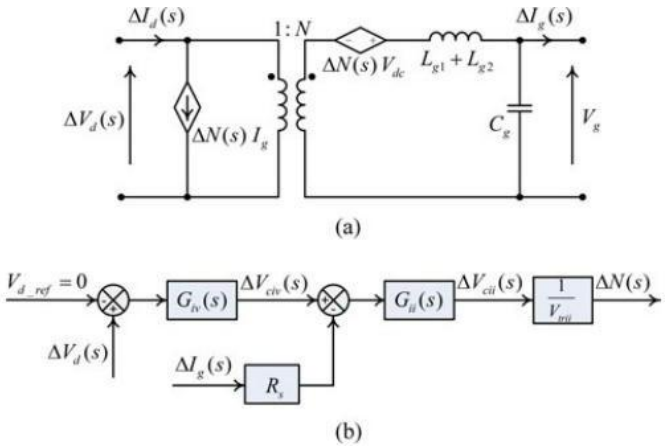


Fig. 5. Modeling of the dc–ac converter. (a) Power stage. (b) Control block Diagram

Where Gb(s) is the transfer function of the controller in the boost converter and Vtrib is the amplitude of the carrier of the PWM modulator.

IV. INDUCTION MOTOR (IM)

An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120 f}{P}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

A. Control Strategy of Induction Motor

Power electronics interface such as three-phase SPWM inverter using constant closed loop Volts l Hertz control scheme is used to control the motor. According to the desired output speed, the amplitude and frequency of the reference (sinusoidal) signals will change. In order to maintain constant magnetic flux in the motor, the ratio of the voltage amplitude to voltage frequency will be kept constant. Hence a closed loop Proportional Integral (PI) controller is implemented to regulate the motor speed to the desired set point. The closed loop speed control is characterized by the measurement of the actual motor speed, which is compared to the reference speed while the error signal is generated. The magnitude and polarity of the error signal correspond to the difference between the actual and required speed. The PI controller generates the corrected motor stator frequency to compensate for the error, based on the speed error.

ISSN 2348 – 8034
Impact Factor- 5.070

V. MATLAB/SIMULATION RESULTS

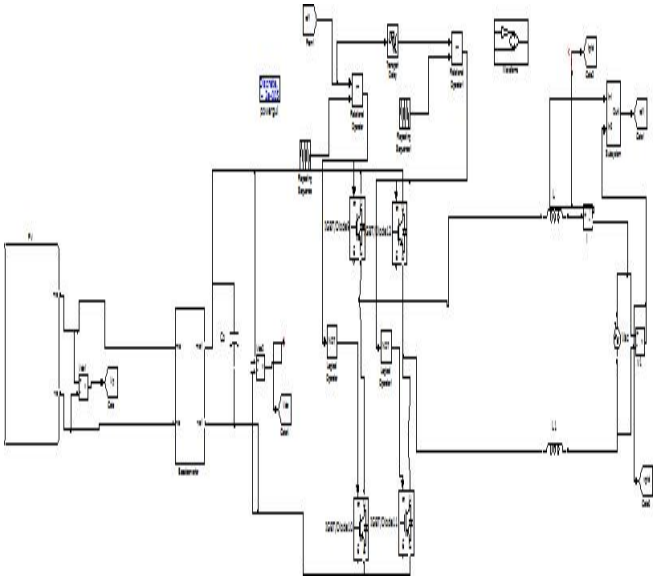


Fig.6 shows the Matlab/Simulink model of proposed converter connected to grid

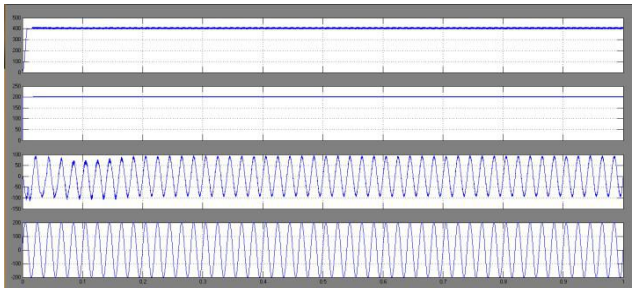


Fig.7 shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under rated condition

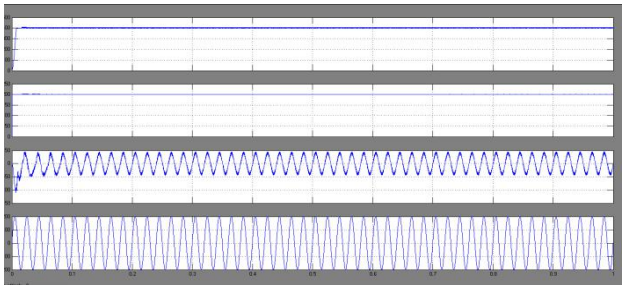


Fig.8 shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 50% of rated condition

ISSN 2348 – 8034
Impact Factor- 5.070

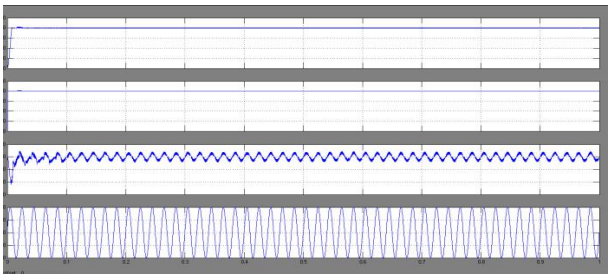


Fig.9 shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 10% of rated condition

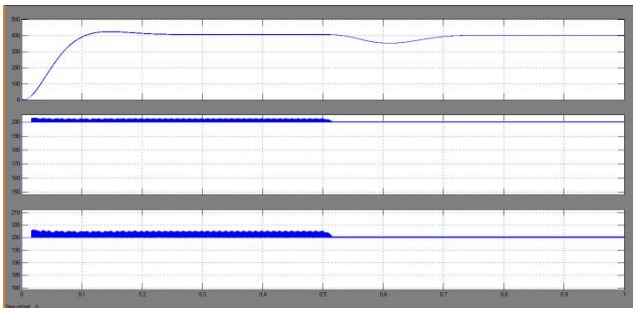


Fig.10 shows the transient response of the system boost voltage Vdc, PV voltage Vpv from full load to 10% load condition

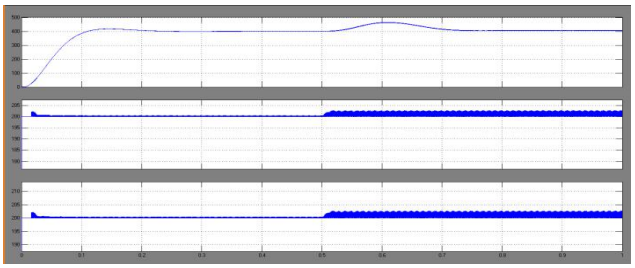


Fig.11 shows the transient response of the system boost voltage Vdc, PV voltage Vpv from 10% load to full load condition

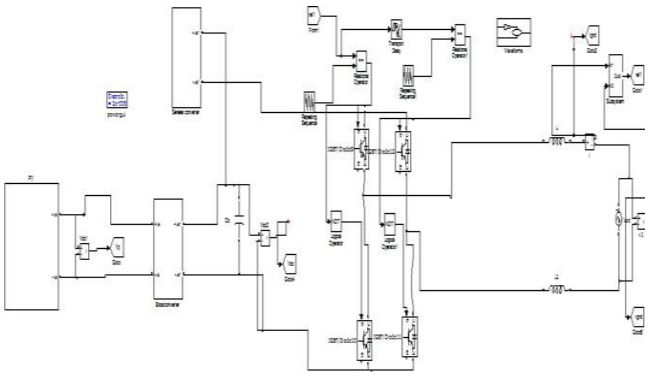


Fig.12 shows the Matlab/Simulink model of proposed converter connected to grid with series voltage compensator

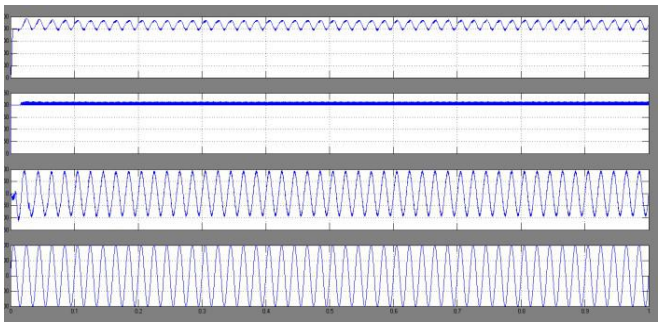


Fig.13 shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under rated condition

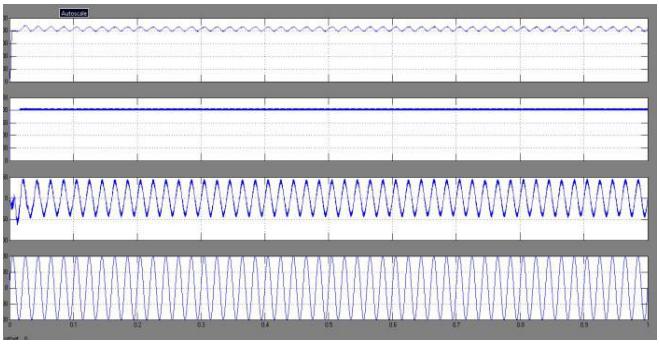


Fig.14 shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 50% of rated condition

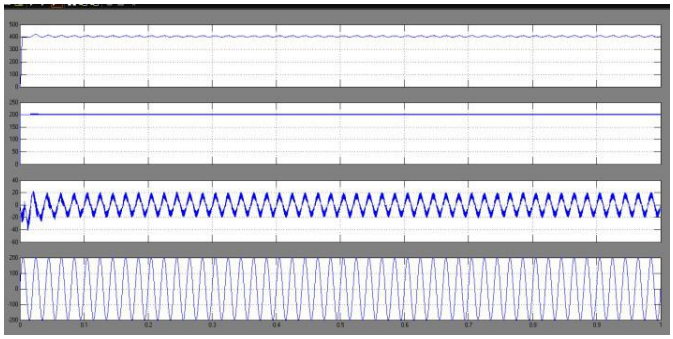


Fig.15 shows the simulation waveforms of boost voltage Vdc, PV voltage Vpv, grid current Ig, grid voltage Vg under 10% of rated condition

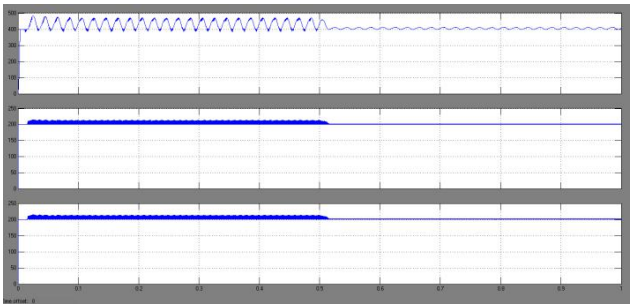


Fig.16 shows the transient response of the system boost voltage Vdc, PV voltage Vpv from full load to 10% load condition

ISSN 2348 – 8034
Impact Factor- 5.070

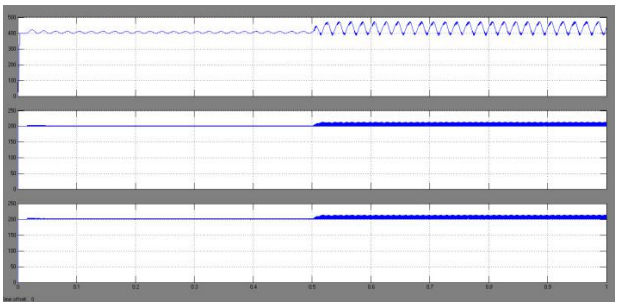


Fig.17 shows the transient response of the system boost voltage Vdc, PV voltage Vpv from 10% load to full load condition

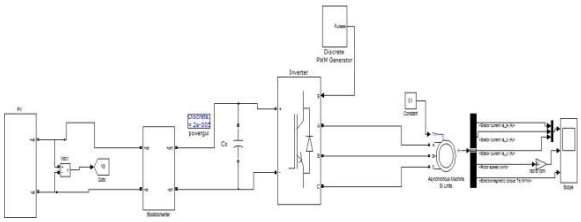


Fig.18 shows the Matlab/Simulink model of proposed converter connected to induction motor system

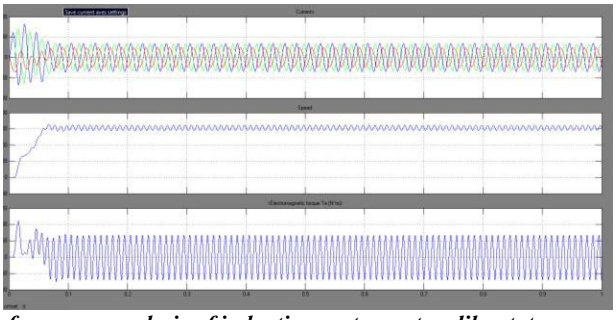


Fig.19 shows the performance analysis of induction motor system like stator current, speed and torque

VI. CONCLUSION

This paper extends the study of the concept proposed,in which a series voltage compensator is used to reduce the dc-link capacitance. Such concept is applied to a grid-tie solar inverter. The modeling and design of the series voltage compensator has been presented.An active series voltage compensator for reducing the dc-link capacitance in a capacitor-supported power electronic system has been proposed. The implementation requires low-voltage devices only, as the dc-link module only handles ripple voltage in the dc-link and reactive power flow in the dc link. A detailed study on the dc and ac characteristics, stability analysis, and hold-up time performance has been given. The design guidelines for the dc-link module for applications with and without the hold-up time requirement have been described. The proposed concept is finally connected to an induction motor system and characteristics are observed.

REFERENCES

[1] Wenchao Liu, Kewei Wang, Henry Shu-hung Chung, Senior Member, IEEE, and Steve Tzu-hsiung Chuang"Modeling and Design of Series Voltage Compensatorfor Reduction of DC-Link Capacitance in Grid-Tie Solar Inverter"IEEE Transactions On Power Electronics, Vol. 30, No. 5, May 2015

[2] A. Braham, A. Lahyani, P. Venet, and N. Rejeb, "Recent developments in fault detection and power loss estimation of electrolytic capacitors," IEEE Trans. Power Electron, vol. 25, no. 1, pp. 33–43, Jan. 2010.

[3] N. Blattau and C. Hillman, "Has the electronics industry missed the boat on Pb-free?–failures in ceramic capacitors with Pb-free solder interconnects," in Proc. 5th Int. Lead Free Conf. Electron. Components

Assemblies, San Jose, CA, USA, Mar. 18–19, 2004.
[4] G. Terzulli, Film Technology to Replace Electrolytic Technology in Wind Power Applications, AVX Technical Note, 2010.
[5] Film Capacitors for Industrial Applications, EPCOS Application Note, EPCOS AG, Munich, Germany, 2007.
[6] S. Harb and R. S. Balog, "Reliability of candidate photovoltaic moduleintegrated-inverter (PV-MII) topologies a usage model approach," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 3019–3026, Jun. 2013.
[7] P. Pelletier, J. M. Guichon, J. L. Schanen, and D. Frey, "Optimization of a DC capacitor tank," IEEE Trans. Ind. Appl., vol. 45, no. 2, pp. 880–886, Mar./Apr. 2009.
[8] D. Lamar, J. Sebastian, M. Arias, and A. Fernandez, "On the limit of the output capacitor reduction in power-factor correctors by distorting the line input current," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1168–1176, Mar. 2012.
[9] I. S. Freitas, C. B. Jacobina, and E. C. Santos Jr., "Single-phase to singlephase full-bridge converter operating with reduced AC power in the DClink capacitor," IEEE Trans. Power Electron., vol. 25, no. 2, pp. 272–279, Feb. 2010.
[10] B. G. Gu and K. Nam, "A DC-link capacitor minimization method through direct capacitor current control," IEEE Trans. Ind. Appl., vol. 42, no. 2, pp. 573–581, Mar./Apr. 2006.
[11] H. Song, D. Oh, K. Nam, and S. Kim, "Method for controlling voltage of DC-link for electric vehicle," U.S. Patent 7 528 566, May 5, 2009.
[12] J. Ying, Q. Zhang, A. Qiu, T. Liu, X. Guo, and J. Zeng, "DC-DC converter circuits and method for reducing DC-bus capacitor current," U.S. Patent 7 009 852, Mar. 7, 2006.
[13] R. X. Wang, F. Wang, D. Boroyevich, R. Burgos, R. X. Lai, P. Q. Ning, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," IEEE Trans. Power Electron., vol. 26,no. 5, pp. 1430–1443, May 2011.
[14] H. B. Li, K. Zhang, and H. Zhao, "Active DC-link power filter for single phase PWM rectifiers," in Proc. IEEE Int. Conf. Power Electron. Asia, 2011, pp. 2920–2926.